Signal integrity in deep-sub-micron integrated circuits

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Outline

• Introduction
  – General signaling scheme

• Noise sources and effects in DSM ICs
  – Supply noise
  – Synchronization noise
  – Cross talk
  – Inter-symbol interference

• Design for signal integrity
  – Power distribution network
  – Clock distribution network
  – Cross-talk immune/aware design
  – Noise margins
  – Binary encodings
Introduction

• Trends in DSM ICs
  – Chip size
  – Component size
  – Supply voltage
  – Voltage threshold
  – Performance

• Communication issues in DSM SoC
  – Routability
  – Performance
  – Power
  – Reliability

Signaling scheme (1)

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Signaling scheme (2)

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Common-mode supply noise

\[ V_{dd} + V_{nd}(t) \]
\[ Gnd + V_{ng}(t) \]
\[ V_{in} \rightarrow V_{out} \]

\[ V_{dd} \]
\[ V_{nd}(t) = V_{ng}(t) = V_n(t) \]

\[ V_n \] directly affects \[ V_{in} \] and \[ V_{out} \]

\[ V_{out} = F(V_{in} - V_n) + V_n \]

\[ t_r \neq t_f \]

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Differential supply noise

\[ V_{dd} + V_{nd}(t) \]
\[ Gnd + V_{ng}(t) \]
\[ V_{in} \rightarrow V_{out} \]

\[ V_{dd} \]
\[ V_{nd}(t) = -V_{ng}(t) = V_n(t) \]

\[ V_n \] affects performance and swing

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Supply noise sources (1)

\[ V_{ddR} = V_{ddT} - Z_d I_d = V_{ddT} - V_n \]
\[ Gnd_R = Gnd_T - Z_g I_g = Gnd_T - V_n \]

[Equation]

\[ V_{out} = F(V_{in} + V_n) - V_n \]
\[ t_r < t_f \]
\[ V_{ltR} = V_{ltT} - V_n \]
\[ t_{p1-0} > t_{p0-1} \]

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Supply noise sources (2)

\[ V_{ddR} = V_{ddT} + Z_d I_d = V_{ddT} + V_n \]
\[ Gnd_R = Gnd_T + Z_g I_g = Gnd_T + V_n \]

[Equation]

\[ V_{out} = F(V_{in} - V_n) + V_n \]
\[ t_{raise} > t_{fall} \]
\[ V_{ltR} = V_{ltT} + V_n \]
\[ t_{p1-0} < t_{p0-1} \]

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Supply noise sources (3)

\[ V_{ddR} = V_{ddT} - Z_d I_d = V_{ddT} - V_n \]
\[ Gnd_R = Gnd_T + Z_g I_g = Gnd_T + V_n \]

\[ t_{raise} = t_{fall} < t_{rf-nom} \]
\[ V_{lt} R = V_{lt} T \]
\[ t_{p1-0} = t_{p0-1} \]

Supply noise sources (4)

\[ V_{ddR} = V_{ddT} + Z_d I_d = V_{ddT} + V_n \]
\[ Gnd_R = Gnd_T + Z_g I_g = Gnd_T - V_n \]

\[ t_{raise} = t_{fall} > t_{rf-nom} \]
\[ V_{lt} R = V_{lt} T \]
\[ t_{p1-0} = t_{p0-1} \]
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Nominal condition
Clock skew

Clock jitter
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Cross talk

\[ C = \frac{K \varepsilon_0 A}{d} \]

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Cross talk (scaling)

Victim
Constant (Gnd)
Aggressor

STM 0.18µm

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<th>W_min</th>
<th>T</th>
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</tbody>
</table>

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Cross talk: floating victim

\[ \Delta V_v = \Delta V_a \cdot \frac{C_c}{C_g + C_c} \]

Cross talk: driven quiet victim

\[ \Delta V_v = \Delta V_a \cdot \frac{C_c}{C_g + C_c} \]

\[ C_a = C_c + C_g \]
Cross talk: switching victim (1)

Cross talk: switching victim (2)
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Inter-symbol interference (ISI): LC

\[ K_{rT} = \frac{Z_r - Z_o}{Z_r + Z_o} \]

\[ K_{rS} = \frac{Z_s - Z_o}{Z_s + Z_o} \]

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Inter-symbol interference (ISI): LC

- $Z_S = 0, \ Z_T = Z_O$
- $Z_S > 0, \ Z_T = Z_O$
- $Z_S < Z_O, \ Z_T = \infty$
- $Z_S = Z_O, \ Z_T = \infty$

Inertial delay: time required by a node/line of a logic circuit to reach its steady state value.

Inter-symbol interference (ISI): RC

- Inertial delay: time required by a node/line of a logic circuit to reach its steady state value.
- There is ISI whenever the cycle time (i.e., the symbol time) is lower than the inertial delay of a node/line.

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Power distribution network

\[
R_p = \frac{I_p r_{n_s}}{2N W_p} \\
A_p = \frac{L_p W_p}{2N k_p} \\
I_{pk} = \frac{C_{dd} Vdd}{t_c} \\
I_p = I_{pk} N_{space} \frac{A_p}{A} \\
V_{drop} = \sum_{i=1}^{N/2} I_p R_p \\
\]

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Clock distribution tree

- Circuit partitioning
- Buffer tree
- Balanced paths
- Meshing
- Transitions:
  - fast for jitter
  - slow for crosstalk

Cross-talk-aware design

- Careful routing
- Regular fabrics
  - Signal
  - Power
  - Ground
- Compensation
  - Symmetric aggressors
- As slow as possible transitions
- Reduced use of floating nodes
Eye opening

Noise margins

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NSR of $V_{Rout}$

Back prop. of NSR from $V_{Rout}$ to $V_{Rin}$
Back prop. of NSR from $V_{\text{Rout}}$ to $V_{\text{Rin}}$

NSR of $V_{\text{Rin}}$

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Limiting bit rate

The bit rate is limited by:
1. the size (and shape) of the NSR of each bit
2. the maximum slope of $V_{Rin}$, determined in its turn by the RC product

Receivers with hysteresis:
Schmitt trigger
Back propagation with hysteresis (1)

\[ V_{H_{\text{min}}} - A_{V_H} + dA_{V_H} + V_{\text{noise}} \]
\[ V_{L_{\text{max}}} + A_{V_{LL}} - dA_{V_{LL}} - V_{\text{noise}} \]

\[ t_0 - T_{\text{prop}} - T_{NS} - T_{NR} - T_{NC} \]

Back propagation with hysteresis (2)

\[ V_{H_{\text{min}}} - A_{V_{HH}} + dA_{V_{HH}} + V_{\text{noise}} \]
\[ V_{L_{\text{max}}} + A_{V_{LL}} - dA_{V_{LL}} - V_{\text{noise}} \]

\[ t_0 - T_{\text{prop}} + T_{NS} + T_{NR} + T_{NC} \]
The bit rate is limited by:
1. the size (and shape) of the NSR of each bit
2. the maximum slope of $V_{\text{Rin}}$, determined in its turn by the RC product

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A physical channel can be used at twice its limiting bit rate to transmit bit streams with no isolated bits.
Bit-level encodings

- **Error-detecting codes**
  - Allow the receiver to detect a given set of random errors on the received stream
  - Possibly combined with re-transmission protocols
- **Error-correcting codes**
  - Allow the receiver to correct a given set of random errors possibly affecting the received stream
- **Low-power encodings**
  - Reduce the average switching activity on long interconnects
- **Constrained encodings**
  - Avoid noise-sensitive conditions and ISI

Bibliography