Charge-based on-chip measurement technique for the selective extraction of cross-coupling capacitances

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Abstract

We present a simple test structure (derived from the CBCM technique proposed by Sylvester et al. \cite{1}) that enables the selective extraction of cross-coupling capacitance between arbitrary on-chip interconnects. We discuss the silicon implementation on a 0.18um CMOS process and report preliminary experimental results.

Introduction

Charge-based capacitive measurements (CBCM) \cite{1} are gaining importance for on chip interconnect capacitance extraction because of their accuracy and simplicity: the transducer is composed of a nmos and a pmos transistor in a pseudoinverter configuration (Fig. 1). The two mosfets are driven by non-overlapping signals ($V_{pu}$ and $V_{pd}$) generated in order to avoid short-circuit current. The overall capacitance $C$ at the output of the pseudoinverter can be extracted by measuring the average current $I$ supplied by the pmos, according to

$$ C = \frac{I}{V_{dd} \cdot f} \quad (1) $$

where $V_{dd}$ is the supply voltage and $f$ is the frequency of the non-overlapping clock signals. Equation (1) holds whenever $f$ is slow enough to allow a complete charge/discharge of $C$ at every cycle.

In general, capacitance $C$ is made of many contributions: drain junctions, mosfet overlapping capacitances, capacitive coupling of the driven net, ... In order to selectively extract a specific contribution (e.g., the cross coupling capacitance between two interconnects, denoted by $C_x$ in Fig. 1), two identical capacitance/current transducers are used with output loads differing only for the coupling capacitance under measure \cite{1}, so that the unknown capacitance $C_x$ can be obtained as $C\!-C_{\text{ref}}$ (the reference pseudoinverter is dotted in Fig. 1). Although in principle each transducer can sense capacitances of the order of attofarad, the accuracy of the differential measures is actually limited by the capacitive mismatch of the two structures ($C_0 \neq C_{\text{ref}}$), which is in the order of fraction of femtofarad for minimum-size pseudoinverters in a 0.18um technology. Increasing the mosfet size would not reduce the mismatch because of charge injection \cite{2}, that is not compensated in a differential measure since it depends on the load capacitance as well. Moreover, guaranteeing the same boundary conditions for the two structures is even harder than matching the inherent parameters of the two pseudoinverters.

A solution to overcome these limitations was proposed by Froment et al. \cite{2}: a single test structure is used (thus avoiding mismatch issues) at the cost of using independent pseudoinverters to drive each wire in the structure under test.

In this paper we propose a simpler technique that exploits crosstalk to measure intra-wire capacitance by means of a single pseudoinverter.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure1.png}
\caption{Differential CBMC structure for cross-coupling measurements \cite{1}. $C_x$ denotes the capacitance under test, $C_0$ the parasitic capacitance, $C_{\text{ref}}$ the reference parasitic capacitance.}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure2.png}
\caption{a) The proposed transducer. b) Schematic representation of signal waveforms and supply currents.}
\end{figure}

The proposed technique

The proposed approach is shown in Fig. 2a. The unknown coupling capacitance $C_x$ is regarded as a crosstalk capacitance between an aggressor (a) and a victim (v). While the victim is driven by the pseudoinverter that acts as a CBCM transducer, the aggressor is driven by a variable voltage source $V_a$ that provides either a constant voltage or a square waveform. Fig. 2b shows the waveforms of $V_{pu}$, $V_{pd}$ and $V_a$ and the corresponding supply current $I$.

The falling edge of $V_{pu}$ causes a current pulse that charges the overall capacitance $C=C_0+C_x$ with an amount of charge $Q=V_{dd}IC$. If a falling transition of $V_a$...
occurs when the pull-up of the pseudoinverter is active, an additional current pulse is supplied to compensate the effect of crosstalk. The corresponding charge is $Q_x = \Delta V_a C_x$, where $\Delta V_a$ is the voltage variation on the aggressor line. On the other hand, a transition of $V_a$ occurring when the pull-down of the pseudoinverter is active and the pull-up is not, doesn’t cause any additional supply current. Hence, if signals $Vpu$, $Vpd$ and $V_a$ are repeatedly applied at frequency $f$, the average measured current is

$$I_{\text{avg}} = fV_d C - f\Delta V_a C_x$$

(2)

where $\Delta V_a$ is the overall variation of $V_a$ during the charge phase. If two experiments are performed with different values of $\Delta V_a$, capacitance $C_x$ can be obtained from

$$I_{\text{avg}}^{(1)} - I_{\text{avg}}^{(2)} = f(\Delta V_a^{(2)} - \Delta V_a^{(1)}) C_x$$

(3)

Mismatch is not an issue, since the same structure is used for both measures. It is also worth noting that the effect of $C_x$ is not masked by the overall capacitance $C$, even if $C_x > C$. In fact, ground coupling reduces the effect of crosstalk in terms of voltage, but it does not mask the effect it terms of charge.

**Implementation and measurements**

The scheme of Fig. 2 has been implemented in a $0.18\mu m$ technology from STMicroelectronics and applied to a simple test structure whose cross-section is shown in Fig. 3. The victim is a M1 line $90\mu m$ long, coupled with two parallel M1 aggressors for a length of $60\mu m$. All lines have minimum width and spacing. Pre-shaping CMOS inverters were added to drive input signals avoiding voltage overshooting possibly occurring during on-wafer measurements. In particular, the pre-shaping buffer on the aggressor line reduces the flexibility in the choice of $V_a$, but increases the accuracy by reducing the uncertainty on $\Delta V_a$, that is now equal to the supply voltage of the buffer.

Accuracy is then limited only by the precision and stability of the external instrumentation: i) the bias voltage generator, ii) the average current meter and iii) the frequency of the input waveforms. We used a semiconductor parameter analyzer (namely, the HP4155) providing voltage uncertainties of hundreds of microvolts (about 0.08% for a $1.8$ supply voltage) and average current measures with a 0.18% error for tens of nA (that could be reduced by increasing the integration time). Additional circuits (of a few logic gates) were integrated to generate non-overlapping input signals $Vpu$ and $Vpd$ from an external clock. In this way a 2-channels pulse generator (namely, an HP8110) was sufficient for driving both the pseudoinverter and the aggressor with a frequency stability of 0.1%.

As an example, for a $1.8$ supply voltage and a clock frequency of $1$MHz, average currents of tens of nA are measured for loads in the range of tens of FF. The operating frequency could be increased to tens of MHz without violating working conditions, but this would prevent the use of standard benches for semiconductor parametric testing. To this purpose, it is worth noting that our test structure is suitable to be implemented between the pad of the scribe line and used also for back-end monitoring in production lines.

**Experimental results**

We applied supply voltages of $1.8$V to both the pseudoinverter and the aggressors. Three different signal waveforms were applied to each aggressor, exhibiting different behaviors during the charge phase of the victim: a) a constant signal (corresponding to $\Delta V_a=0$), b) a rising transition (corresponding to $\Delta V_a=V_{dd}$), and c) a falling transition (corresponding to $\Delta V_a=-V_{dd}$). Measurements were performed for different combination of the operating conditions of the two aggressors ($60\mu m$ coupling case):

$$\Delta V_{a1} \Delta V_{a2} \quad I \quad \text{Measure [A]}$$

| (aa) | 0 | 0 | $V_{dd}(C_0+2C_x)$ | 3.1645E-08 |
| (ab) | 0 | $V_{dd}$ | $V_{dd}(C_0+C_x)$ | 2.1240E-08 |
| (ac) | $-V_{dd}$ | $V_{dd}$ | $V_{dd}(C_0+3C_x)$ | 4.1509E-08 |
| (ba) | $V_{dd}$ | 0 | $V_{dd}(C_0+C_x)$ | 2.1200E-08 |
| (bb) | $V_{dd}$ | $V_{dd}$ | $V_{dd}(C_0+C_x)$ | 1.1304E-08 |
| (ca) | $-V_{dd}$ | 0 | $V_{dd}(C_0+3C_x)$ | 4.1520E-08 |
| (cc) | $-V_{dd}$ | $-V_{dd}$ | $V_{dd}(C_0+4C_x)$ | 5.1840E-08 |

All measured average currents provide different equations to extract $C_x$ and its multiples. For instance, $C_x=(I_{\text{avg}}(aa)-I_{\text{avg}}(ab))/V_{dd}$ or $C_x=(I_{\text{avg}}(ac)-I_{\text{avg}}(ba))/V_{dd}$; $2C_x=(I_{\text{avg}}(aa)-I_{\text{avg}}(bb))/V_{dd}$ or $2C_x=(I_{\text{avg}}(ac)-I_{\text{avg}}(ab))/V_{dd}$. This allows us to check the accuracy and robustness of the proposed approach. Experimental results are shown in Fig. 3 for two test structures (with $30\mu m$ and $60\mu m$ couplings between M1 wires), where the unknown capacitance is the slope of the regression equation. The high linearity ($r=0.9999$) demonstrates the validity of the technique. For the $60 \mu m$ test structure, the slope (i.e., the coupling capacitance) is 5.634fF, with a ±0.2% accuracy. More test structures are currently under development to check the accuracy of the approach. After accuracy assessment, the approach will be systematically applied to measure cross coupling capacitances of interconnects in deep sub micron integrated circuits. Measures will then be used for model characterization/validation and in-line process monitoring.

**References**
